ABSTRACT

In this final project, the FIR filter has been designed with equiripple method which will occur over a bandwidth of 40 Mhz at a frequency of 50-90 Mhz and realized on FPGA. This FIR filter is implemented to be used on the ISL (*Inter Satellite Links*). This FIR filter method been selected because the communication that conducted on ISL is a data communication. Data communication required a linear phase response, whereas the filter that can guarantee a linear phase response is a FIR Filter.

Equiripple method is taken because this method is the most reliable and the most optimal due to approaching the magnitude of errors between the desired frequency responses to the actual frequency responses which spreads evenly in the passband and stopband so it can minimize the magnitude of errors. The design of this FIR filter is conducted with theoretical calculations and using R2012b matlab simulation program. In order to implement it, used FPGA with a VHDL as the programming language with a help of Xilinx ISE Design Suite 14.5

The design of FIR filter orde is 272. FIR filter digital implemented in FPGA GENESYS Xilinx Virtex-5 XC5VLX50T with resource FPGA : number of slice register 13%, number of slice LUT 39%, NUmber of bonded IOb 3%, number of BUFG/ BUFGCTRLs 9%, number of PLL_ADV 16 %, and number of DSP48 93%. *Bandwidth* is 40-90Mhz, and the phasa response is linear.

Keywords: *Filter FIR, equiripple, FPGA, VHDL*