ABSTRACT

Low Density Parity Check or LDPC is one of channel coding technique which was developed by Robert G. Gallager in 1962. LDPC is known for its capability as the nearest channel coding technique for reaching maximum of Shannon Capacity. Therefore, LDPC is suitable to use for high data rate and high channel noise. LDPC is known for its low complexity for implementation as well.

This final project purposes were designing architectural of LDPC code system and implementing LDPC code system on FPGA Cyclone II board. The error correction which was used for this project was message passing algorithm. Two types of code rates were used for implementation. The code rates were ½ and ¾. Code rate ½ used matrix 4x8, matrix 8x16, and matrix 24x48. Code rate ¾ used matrix 4x16.

The results showed that the systems could be implemented on FPGA Cyclone II board. The message passing algorithm could do error correction process for more than one bit error. The frequency of matrix 4x8 systems was 1,35 MHz. The frequency of matrix 8x16 systems was 0,909 MHz The frequency of matrix 24x48 systems was 0,156 MHz. The frequency of matrix 4x16 systems was 1,35 MHz.

Keywords *: Code rate*, FPGA Cyclone II, *LDPC, message passing*