ABSTRACT

IFFT (Inverse Fast Fourier Transform) is a computational algorithm which is an inverse of FFT (Fast Fourier Transform). The IFFT method serves as an algorithm to speed up calculations from IDFT (Inverse Discrete Fourier Transform). With the IFFT, the calculation of IDFT can be significantly reduced so the calculation becomes simple and efficient in its implementation. Some of the implementation is in the field of health, navigation, telecommunications, sound processing.

In this final project, the author has designed the 64 point IFFT system using the radix-4 algorithm and successfully implemented on FPGA Altera Cyclone II - EP2C20F484C7. This implementation aims to prove whether the design of this system can be designed on FPGA hardware. This system is designed using VHDL, which is a language that aims to encode the blocks of a system that has been created. This design simulation uses MODELSIM as a pre-implementation treatment to FPGA hardware. The simulation results will be compared with the simulation on MATLAB and manual calculations in Microsoft Excel.

After the simulation is done and the results are obtained, it is continued by synthesizing the VHDL design into FPGA Altera Cyclone II - EP2C20F484C7 using Programmer features in Quartus software. The total number of resources required from the synthesis result is total logic elements, total combinational functions, dedicated logic registers totaling, total pins totaling, total memory bits, and embedded multiplier 9-bit elements. These results indicate that the IFFT 64 point system using radix-4 algorithm can be implemented to FPGA Altera Cyclone II - EP2C20F484C7.

Keywords : IDFT, IFFT, VHDL, FPGA