ABSTRACT

DCT is a data transform that converts from time domain to frequency domain, it capables to separating informations from low frequency to high frequency. The benefits of this data transform quite a lot, because with the help of this data transform can reduce the amount of data contained by the image without damaging the image's quality.

In this final project the author has designed DCT system with N = 8 and N = 2 and successfully implemented on FPGA Altera Cyclone II - EP2C20F484C7. This study aims to prove that DCT can be implemented on FPGA and the result is not much different from the calculation using MATLAB. This system is designed using VERILOG language which is a hardware language dimeringrti by FPGA, this language selection to facilitate in coding calculation of DCT system. The system is encoded using Quartus Lite 16.0.0.2.1.1 and simulated with MODELSIM and then synthesized on FPGA. The output of the FPGA will be compared with the output of MATLAB.

Once simulated and obtained the result, the system is synthesized to the Altera Cyclone II FPGA board - EP2C20F484C7. From the simulation results that can be implemented on the Altera Cyclone II FPGA board - EP2C20F484C7 only DCT with N = 2 because DCT with N = 8 consumes a large resource memory of 3285% while the DCT system with N = 2 is 92%. From the simulation results also obtained comparison of time delay and BER between calculations using MATLAB and FPGA. The result is the time delay required by MATLAB to calculate DCT with N = 8 is 0.10894 s and with N = 2 is 0.12107 s whereas the time required by FPGA to calculate DCT with N = 8 is 0.00000024 s and with N = 2 is 0, 00000136 s. The BER produced between MATLAB and FPGA is 0.2930 for DCT with N = 2 and 0.0503 for DCT with N = 8.

Keywords: ***Discrete Cosine Transform, Image Compression, Field Programmable Gate Array.***