ABSTRACT

In computing systems, high-speed processors rely on mathematical operations. Mathematical operations are part of the main hardware block of most digital signal processing systems. Multiplication is basic mathematical operation that dominates the processor execution time when compared to other operations. This paper presents high-speed 8x8 bit multiplication technique that is very different from conventional multiplication systems, since the proposed method is based on Vertical and Crosswise structures of Vedic mathematics. Vedic Mathematics facilitates some solutions to some extent. The proposed multiplication system using Vedic math is encoded in VHDL (Very High Speed Integrated Circuit Hardware Description Language) and implemented using the Altera DE-1 FPGA board. The results of the analysis and implementation are compared with conventional multiplication method and Booth radix-4 method to show significant efficiency improvement in time delay. The delay time is reduced by 1,231 clock for slow model and 0,413 clock for fast model compared to the delay time if using conventional methods.

***Keywords**: Vedic Mathematic, VHDL, multipliers, FPGA, delay, Ripple Carry Adder, architecture.*