ABSTRACT

FFT (Fast Fourier Transform) is a method of discrete signal solving which is used at present. One of the significant usages is in OFDM technology. Since FFT is used, it is only viewed as a computation system. In this research, there will be hardware architecture of 64 points FFT in order to make easier in using it, so that there will be more technology which applies FFT.

This research used VHDL as the language which coded every block in this 64 points FFT system. The design with VHDL would give the system a model which matched with the need of 64 points FFT system and would simulate it with ModelSim before the software synthesize translated the design in hardware. From the result of modeling simulation, there would be synthesize at the hardware FPGA level with Xilinx Synthesize Tools.

The input of 64 points FFT system made was the output of IFFT system, while the output in the form of discrete signal was the input of IFFT. From the synthesize result there would be number of slices and another parameters which included number of IOB, LUT, Flip-Flop, GCLK, FIFO/RAM and DSP. As a whole, this research was able to proof that the output of FFT matched with the input of IFFT. The minimum period needed in this 64 points FFT system was 14.136ns, and the maximum frequency was 70,741 MHz.

Key Word : DFT, FFT, VHDL