ABSTRACT

The method of IFFT is the inverse or the opposite of FFT, in which FFT is a method to solve the discrete signal. IFFT is a quick computational algorithm to count IDFT. The sub carrier in IFFT has a rounded common multiple harmonize frequency of it basic frequency as well as Fourier row component in composite signal. One of the IFFT usages is the OFDM system; in here IFFT has the role as the modulator in transmitter.

In this research, it would be made a hardware structure design of IFFT by coding every block in IFFT by using VHDL language. The system design with VHDL would give a model of system which matched with the need of IFFT system and simulated before the synthesize tools translated the design in hardware as a real with ModelSim as support software. From the result of modeling and simulation there would be synthesize at the hardware FPGA level with Xilinx.

As the input of IFFT was the discrete signal as the output of quantizer, and from the output there would be diskrit signal in time domain. In here, it was hoped that the output of IFFT could be seen. The result of the implementation in FPGA would be analyzed its performance which included: the design result of parameter performance, number of slice needed, process of delay and the success of algorithm to count IFFT.