A B S T R A C T

Video data has high bit rate,it needs to be compressed in order to reduce the data rate of a video sequence so it can be transmitted real-time trough existing communication channel. The video compression scheme used is intra frame compression that refers to ITU-T standard H.263 used for video-conferencing and video-telephony applications in low bit rate.

In this final project, has an objective of encoding, transmission, reception, and subsequent decoding of grayscale video image with size 128 x 96 pixel. The Encoder receives blocks of 8x8 pixel data from the USB web camera connected with Linux PC and displays the real-time video image result on VGA monitor.

The HDL design used Active-HDL 3.5 software and synthesized with Foundation Project Manager 2.1i software and hardware implementation target on FPGA Xilinx XC4010XL-PC8403. Result from the implementation required 76% CLB (307 out of 400), with maximum frequency may used is 14.862 MHz for the encoder part and required 100% CLB (400 out of 400), with maximum frequency may used is 11.053 MHz for the decoder part.