Abstract

One of CC-NUMA problem is CC-NUMA system performance itself as well as issues related to the cache and memory. CC-NUMA has implemented a cache coherence and cache coherence protocols that will be used is MOESI CMP Token. Although CC-NUMA has implemented a cache coherence, cache misses in CC-NUMA is not completely gone, just reduced. This is why research needs to be done on the CC-NUMA associated with cache and memory performance.

Another factor that played a role in influencing the cache miss is cache block size. By using different block cache size is 16, 32, 64 and 128 bytes, will be used as a comparison performance CC-NUMA systems. Performance measurement metric is execution time, simulation time, the host instruction rate, the host tick rate, latency, throughput, bandwidth, cache miss rate, and average memory access time.

With larger cache block size on CC-NUMA shows almost all performance parameters except latency and throughput were increased. But the most important parameter minimize the cache miss rate. Overall L1 I, L1 D, L2 cache miss rate were decreased from 39.08% to 8:06% of the cache block size of 16 to 128 bytes. With the addition of the cache block size then the performance of CC-NUMA systems will increase, particularly in the cache and memory performance.