ABSTRACT

Processor is one of main block of a computer system that controls and processing the flow of data. Soft processor is a processor that can be synthesized, programmed, and simulated by programming language so that later it can be planted in a reprogrammable micro semiconductor chip like FPGA technology.

OpenRISC 1200 (OR1200) is a soft processor that the architecture itself is now being developed by opencores.org community. Architecture of OR1200 is an implementation of the open source architecture of OpenRISC 1000 under GNU Lesser General Public License (LGPL). OpenRISC Reference Platform System-on-Chip (ORPSoC) is an architectural platform that can implement OpenRISC.

Field Programable Gate Array (*FPGA*) is an *Integrated Circuit* (*IC*) that can be reprogrammed as we need. This characteristic of FPGA make it has more benefit from other IC product, which is low cost to reprogrammed in case of bugs.

This final project explains about designing and implementing process of general architecture of openRISC 1200 soft processor in System-on-Chip in FPGA. System is running on FPGA Xilinx Spartan-6 LX45 board Atlys™. It can be seen by doing a test, which is to run a simple application program to count prime numbers. And the outputs from FPGA are the same as the outputs from simulation process. And the simulation process itself shows that OpenRISC is running the application by using standard ISA of OpenRISC.

As the synthesize process on FPGA, the resources that OpenRISC processor needed to be implemented in FPGA as follows: 4379 number of slices, 6721 number of flip-flop's slices, 12534 number of LUTs's slices.

Keywords : *OpenRISC, SoC, FPGA, Spartan-6, Atlys.*