## **ABSTRACT**

PID Controller (Proportional Integral Derivative) is a type of control that are common in the world of engineering control. Basically, the PID controller is a simple application of the principle of feedback. The principle of feedback focuses on re-checking the output generated by the system. The resulting output will be compared with the input (set point) and the expected results of the output can approach or even equal to the input value. PID controllers have the ability to eliminate steady state error through the action of the integral controller and gives the effect of damping on the oscillating system by using derivative controllers.

In this final projects, the FPGA becomes the basis for the system to process the data. After that, the coding is done by using the language VHDL (Very High Speed IC Hardware Description Language). Digital PID system is implemented with the basic logic circuit consists of three major series. Summing circuit is the circuit of adder, multiplier, and delay. Graphs the response time acquired by daqboard/1005 with the help of matlab simulink software.

Set point of the voltage from 0 to 5 Volt regulated with a potentiometer. Testing is done with the input voltage of 1.02 volts with a value of Kp (Proportional Constant), Ki (Integral Constant), and Kd (Derivative Constant) different. The results obtained processing the digital PID response approaches the set point with a value of Kp = 27, Ki = 8, and Kd = 10and the error value of about 0.02 volts so as to fix the PID error before being approximately 2.504 volts with a delay time 0.347 seconds. From the results of testing the value of Kp, Ki, Kd obtained a different conclusion that the greater the value of Kp which makes the system steady state error gets smaller. Ki values which make the oscillation system is growing more and more and more to make the system unstable and highly influence the system response. Kd values give a very small effect on system response.

Keywords: PID, Proportional, Integral, Derivative, FPGA, VHDL