ABSTRACT

Multipliers are key components of many high-performance systems such as FIR filters, Microprocessor, digital signal processors, etc. A systems performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Thus, it needs more efficient design for lower the delay for better performance on the system.

The writer then designs one of the fast multiplication of binary data called Booth's Algorithm or Booth's Multiplication. The writer uses the modification method, which is Booth radix-4. The research involves analyse the system by testbench and will be implemented in FPGA Altera DE-1. Writer will analyse the delay and used resource of the system.

The success parameter is to design better performance of binary multiplier compared to other method and conventional method.

KEYWORDS: *FIR Filter, multiplier, Booth's Algorithm, Booth's Multiplication, Booth radix-4, FPGA.*