

DAFTAR PUSTAKA

- [1] [1] B. A. Araujo, G. Gracioli, T. Kloda, D. Hoornaert, and M. Caccamo, "Implementation and Evaluation of Adaptive Cache Insertion Policies for Real-Time Systems," in Brazilian Symposium on Computing System Engineering, SBESC, IEEE Computer Society, 2021. doi: 10.1109/SBESC53686.2021.9628309.
- [2] Bugnion, E., Devine, S., Rosenblum, M., Sugerman, J., & Wang, E. Y. (2012). Bringing virtualization to the x86 architecture with the original vmware workstation. *ACM Transactions on Computer Systems (TOCS)*, 30(4), 1-51.
- [3] FEBRIANI, Shafira; KARNA, Nyoman Bogi Aditya; NUGRAHA, Ramdhan. Analisis Performansi Enkripsi Pada Prosesor Intel Dengan Arsitektur X86. *E Proceedings of Engineering*, 2020, 7.1.
- [4] Hadiwinata, "Hit, Miss, Hit Rate dan Miss Rate Pada Cache," <https://prezi.com/mditiquwqxaf/hit-miss-hit-rate-dan-miss-rate-pada-cache/?fallback=1>, Mar. 2015.
- [5] Id Webhost, "Mengenal Apa Itu Cache Memory dan Perbedaannya dengan Cookies," pp. 2023–02, 2022.
- [6] Intel Expands Mobile Leadership, Brings Enthusiast Performance to Thin-and-Light Laptops., intel. Accessed: Oct. 02, 2023. [Online]. Available: <https://www.intel.com/content/www/us/en/newsroom/news/enthusiast-performance-thin-light-laptops.html>
- [7] M. Qureshi, A. Jaleel, Y. Patt, S. C. Steely Jr, J. Emer, and G. Tech, "RETROSPECTIVE: Adaptive Insertion Policies for High-Performance Caching." [Online]. Available:
- [8] Mahad, Fairus Safwan., & Wan Kadir, Wahn Mohd. Nasir (2013). Improving webserverperformance using two-tiered webcache. *Journal of Theoretical and Applied Information Technology*, 52(3), 243–251
- [9] S. Sethumurugan, J. Yin, and J. Sartori, "Designing a Cost-Effective Cache Replacement Policy using Machine Learning."
- [10] Seiler, L., Carmean, D., Sprangle, E., Forsyth, T., Abrash, M., Dubey, P., ...

- & Hanrahan, P. (2008). Larrabee: a many-core x86 architecture for visual computing. *ACM Transactions on Graphics (TOG)*, 27(3), 1-15.
- [11] Siti Noviah, "Cache Memory Adalah: Tipe, Fungsi dan Cara Kerjanya," pp. 2022–2023, Dec. 2022.
- [12] W. Xiong, S. Katzenbeisser, and J. Szefer, "Leaking Information Through Cache LRU States in Commercial Processors and Secure Caches," 2021.
- [13] X. Zhang, C. Li, H. Wang, and D. Wang, "A cache replacement policy using adaptive insertion and re-reference prediction," in *Proceedings - 22nd International Symposium on Computer Architecture and High Performance Computing, SBAC-PAD 2010*, 2010, pp. 95–102. doi: 10.1109/SBAC-PAD.2010.21.
- [14] Y. Wang, Y. Yang, C. Han, L. Ye, Y. Ke, and Q. Wang, "LR-LRU: A PACS-Oriented Intelligent Cache Replacement Policy," *IEEE Access*, vol. 7, pp. 58073–58084, 2019, doi: 10.1109/ACCESS.2019.2913961.