ABSTRACT

This research focuses on the implementation and performance evaluation of the Bimodal Insertion Policy (BIP) cache replacement policy on the x86 architecture. The x86 architecture is widely used in various computer devices, and cache memory has an important role in increasing data access speed. BIP is an efficient cache management algorithm that uses a binary search tree to keep track of recently accessed cache blocks within each set. The aim of this research is to implement Bimodal Insertion Policy (BIP) on the x86 architecture and measure its performance in terms of cache replacement efficiency. This study includes a literature review of computer architecture, cache memory, and cache replacement policies. The research methodology involves simulation-based experiments using the gem5 simulator. The findings from this research will contribute to the understanding of cache management algorithms and their impact on the efficiency of computer systems.

Keywords: Bimodal Insertion Policy (BIP), x86 architecture, cache memory, cache replacement policy, cache replacement efficiency, gem5 simulator.