ABSTRACT

Telecommunication system purpose to transmit signal from information source / transmitter which is like voice, short message service, image, video and data service to the destination or receiver. The information who will be transmitted, will be changed into signal who can be passed by transmision medium, and in order that received signal can be read, we need a demodulator which is can change received signal into the information like a transmitted signal. Demodulator 64-Quadrature Amplitude Modulation (QAM) is one of the type of demodulator who can demodulate signal in high frequency.

In this thesis has ever been designed and implementated demodulator 64-QAM on FPGA (Field Programable Gate Array) by using programable language Very High Speed Integrated Cicuit (VHSIC) Hardware Description Language (VHDL). In this thesis has ever been implementated sub block from demodulator, such as demapper. The function of this block is to remapped input symbols with the different amplitude and phase who have been representated in to the information bits, but still in the inphase and quadrature bits.

The result of this thesis has been gotten output in the receiver for ideal condition is information bits which is same like an information bits in the transmitter side. When there is some errors, the output bits is same with input bits during the noise just intefere six bits from LSB (Least Significant bit, but for seven bits that are intefered there is 21,8310% error process, whereas fourteen bits that are interfered there is 96,9072% error process.

Keywords : 64-QAM, Digital Demodulation, FPGA, VHDL.