Abstract

In designing phase of embedded system designing using hardware description language (HDL), some characteristics may differ due to using different HDL. That is why it is necessary needed to compare those characteristics between two different HDL, which is, in this final assignment, between SystemC and Verilog. The comparison is done in an implementation of a single-purpose processor with least common multiple (LCM) functionality, in which, compared parameters are latency, memory consumption, runtime delay, and harddisk allocation. There are some steps which should be done, LCM modeling using state-machine modeling, optimation (only if needed), creating diagram block, and implementing it into SystemC and Verilog language, and finally, calculating each compared parameter.

In this research, we found several strengths and weaknesses, such as Verilog's ability in defining clock timing for controller is better than SystemC's one, and vice versa, SystemC's ability is better in flexibility term than Verilog's one.

Keywords: systemc, LCM, verilog, single-purpose processor